REMARKS

Claims 1-21 are pending in this application. By this Amendment, Applicants amend claims 1, 13 and 14.

The drawings were objected to for allegedly failing to show every feature of the invention specified in the claims (particularly, the printed circuit board and the conductive bond recited in claim 13). Applicants have amended claim 13 to remove the recitation of the circuit board. Regarding the conductive bond, the Examiner's attention is directed to Figure 3, and the paragraph bridging pages 14 and 15 of the present application. Reference numerals 11 and 12 are disclosed as being solder. Applicants respectfully submit that the solder 11 and 12 clearly illustrates the "bonding portion defined by a conductive bond is located inside of an outer periphery of the chip electronic component as seen from the top of the chip electronic component" recited in claim 13 of the present application. Accordingly, Applicants respectfully request reconsideration and withdrawal of this objection

Claims 1, 2, 6-12, 14-18, 20 and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kaida et al. (U.S. 5,627,425). And claims 3-5, 13 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kaida et al. in view of Okamura (U.S. 5,892,415). These rejection are respectfully traversed.

Claim 1 recites:

> "A chip electronic component comprising:
> a body having outer peripheral surfaces including an upper surface, a lower surface and a pair of side surfaces;
> an electronic component element having electrodes and being included in said body; and
> **a plurality of external electrodes arranged to extend over at least the lower surface and at least one of the side surfaces of said body of the chip electronic component and electrically connected to the electrodes of the electronic component element; wherein**
> **each portion of said external electrodes provided on the lower surface of said body of the chip electronic component is provided with a narrow portion and a wide portion.**" (Emphasis added).

Claim 14 has been amended to recite features that are similar to the features

recited in claim 1, including the emphasized features.

The present claimed invention provides a chip electronic component that is not susceptible to stress caused by warpage of the substrate on which it is mounted, thereby ensuring a reliable electronic connection and a strong mechanical bond. These advantages are achieved by providing external electrodes on the outer surface of the body of the chip electronic component, arranged to extend over the lower surface and at least one of the side surfaces of the body of the chip electronic component and electrically connected to the electrodes of the electronic component element, wherein each portion of the external electrodes provided on the lower surface of the body of the chip electronic component is provided with a narrow portion and a wide portion.

The Examiner alleges that "Kaida et al. discloses a circuit having a lower surface, a pair of side surfaces, a plurality of external electrodes 117, 118 and external electrode portions provided on the lower surface of the electric component with a narrow portion and a wide portion (see figure 38). . . . Moreover, the width of the external electrode portion on the lower surface of the electronic component element is larger than the width of the external electrode portion formed on the side surface of the electronic component element (see figure 39)."

Further, in the "Response to Arguments" section of the Office Action, the Examiner refers to a completely different portion of Kaida. Particularly, the Examiner alleges that "Kaida et al. discloses a piezo resonator 42, external electrodes 48a which have a conductive part 47a which is narrower and forms part of the electrode (see figure 10). Moreover, in figure 36(a), Kaida et al. discloses an external electrode 48a, which has a narrow portion and a wider portion 82a." Applicants respectfully disagree.

In contrast, Kaida teaches, in Fig. 10, that a resonator 42 is connected to **internal** terminal electrodes 48a and 48b via **internal** conductive parts 47a and 47b. Additionally, Kaida teaches **external** electrodes 117 and 118 which are provided on the outer surface of the component 110, as seen in Fig. 39. As the terminal electrodes 48a, 48b and conductive parts 47a, 47b are provided within the **interior** of the component, as seen in Fig. 38, and elsewhere in Kaida, these elements cannot be properly

construed as "a plurality of external electrodes **arranged to extend over at least the lower surface and at least one of the side surfaces of said body of the chip electronic component and electrically connected to the electrodes of the electronic component element**" (Emphasis added).

The only elements taught in Kaida that are provided on an outer surface of the component and extending to a lower surface of the electronic component element are external electrodes 117 and 118, and neither of the external electrodes 117 and 118 includes "said each external electrode portion provided on the lower surface of the electronic component element is provided with a narrow portion and a wide portion" as recited in claims 1 and 14 of the present application. In contrast, the portions of the external electrodes 117 and 118 provided on the lower surface of the electronic component of Kaida have a constant width along the entire lower surface of the electronic component, and do not include a narrow portion and a wide portion.

Okamura is relied upon merely to teach electrodes having various shapes, and clearly fails to teach or suggest "a plurality of external electrodes arranged to extend over at least the lower surface and at least one of the side surfaces of said body of the chip electronic component and electrically connected to the electrodes of the electronic component element; wherein each portion of said external electrodes provided on the lower surface of said body of the chip electronic component is provided with a narrow portion and a wide portion" are recited in claims 1 and 14 of the present invention. Accordingly, Applicants respectfully submit that Okamura fails to cure the deficiencies of Kaida described above.

Therefore, Applicants respectfully submit that Kaida et al. and Okamura, taken individually or in combination, fail to teach or suggest the unique combination and arrangement of elements recited in claims 1 and 14 of the present application.

In view of the foregoing, Applicants respectfully submit that claims 1 and 14 are allowable. Claims 2-13 and 15-21 are dependent upon claims 1 and 14, respectively, and are therefore allowable for at least the reasons that claims 1 and 14 are allowable.

In view of the foregoing Remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are respectfully solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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VERSION WITH MARKINGS SHOWING CHANGES MADE

1. A chip electronic component comprising:

[a circuit;]

a body having outer peripheral surfaces including an upper surface, a lower surface and a pair of side surfaces;

an electronic component element having [a lower surface and a pair of side surfaces] electrodes and being included in said body; and

a plurality of external electrodes arranged to extend over at least the lower surface and at least one of the side surfaces of said body of the chip electronic component [element] and electrically connected to the [circuit therein] electrodes of the electronic component element; wherein

[said] each portion of said external electrodes [portion] provided on the lower surface of said body of the chip electronic component [element] is provided with a narrow portion and a wide portion.

13. A mounting structure of a chip electronic component according to claim 1 [to be mounted on a printed circuit board via a conductive bond], wherein a bonding portion defined by a conductive bond is located inside of [the] an outer periphery of the chip electronic component as seen from the top of the chip electronic component.

14. A chip electronic component comprising:

[a circuit;]

a body having outer peripheral surfaces including an upper surface, a lower surface and a pair of side surfaces;

an electronic component element having [a lower surface and a pair of side surfaces] electrodes and being included in said body; and

a plurality of external electrodes arranged so as to extend over at least the lower surface and at least one of the side surfaces of said body of the chip electronic

component [element] and electrically connected to the [circuit therein] electrodes of the electronic component element;

wherein each portion of said external electrodes [portion] provided on the lower surface of said body of the chip electronic component [element] is arranged to have an almost uniform width from one longitudinal end to the other, and [satisfies] satisfy the relation $L_1<L_3$, where L_3 is the width of each portion of the external electrodes [portion] provided on the lower surface of said body of the chip electronic component [element], and L_1 is the width of each portion of the external electrodes [portion formed] provided on the at least one side surface of said body of the chip electronic component [element].